Abstract

We disclose the structure of a JFET device, the method of making the device and the operation of the device. The device is built near the top of a substrate. It has a buried layer that is electrically communicable to a drain terminal. It has a body region above the buried layer. A portion of the body region contacts a gate region connected to a gate terminal. The device has a channel region, of which the length spans the distance between the buried layer and a source region, which projects upward from the channel region and is connected to a source terminal. The device current flows in the channel substantially perpendicularly to the top surface of the substrate.